REMARKS

Applicant respectfully requests reconsideration of this application as amended.

Office Action Rejections Summary

Claims 1 – 5, 7 – 14, 16 and 17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,150,223 to Chern et al. (hereinafter "Chern") in view of U.S. Patent 5,976,991 to Laxman et al. (hereinafter "Laxman"). Claims 15, 18 and 19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Chern and Laxman and further in view of U.S. Patent 6,235,597 to Miles (hereinafter "Miles").

Status of Claims

Claims 1 – 5 and 7 – 19 remain pending in the application. Claims 1 and 11 have been amended. The amendments are supported by the specification and no new matter has been added. No new claims have been added. No claims have been canceled.

Rejections Under 35. U.S.C. § 103(a)

Claims 1 – 5, 7 – 14, 16 and 17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Chern in view of Laxman. Applicant respectfully submits that claims 1 – 5, 7 – 14, 16 and 17 are patentable over Chern and Laxman.

Amended independent claim 1 provides:

> A method of forming sidewall spacers adjacent opposing vertical sides of a gate electrode, comprising:
> forming at least one gate electrode over a substrate;
> forming, at a first temperature in a range of approximately 550°C to 580°C and a first pressure of about 10 mTorr, a first silicon oxide film conformally over the substrate and gate electrode from a combination of gases including bis-(tertiarybutylamino)silane and oxygen;
> forming, at ***a second temperature in a range of 580°C to less than 600°C and a second pressure of about 65 Pascal,*** a silicon nitride film conformally over the first silicon oxide film from a combination of gases including bis-(tertiarybutylamino)silane; and
> forming a second silicon oxide film over the silicon nitride film from a combination of gases including bis-(tertiarybutylamino)silane and oxygen;

wherein the first temperature is less than the second temperature.

(emphasis added)

Amended independent claim 11 provides:

> A method of forming a transistor, comprising:
> forming at least one gate electrode over a gate dielectric layer, the gate dielectric layer disposed on a substrate;
> depositing a first silicon oxide film conformally over the substrate and gate electrode from a combination of gases comprising bis-(tertiarybutylamino)silane and oxygen at a first temperature of between approximately 550°C and 580°C and a pressure of about 10 mTorr;
> depositing a silicon nitride film conformally over the first silicon oxide film from a combination of gases comprising bis-(tertiarybutylamino)silane and ammonia at ***a second temperature of between 580°C and less than 600°C and a second pressure of about 65 Pascal***;
> depositing a second silicon oxide film over the silicon nitride film from a combination of gases comprising bis-(tertiarybutylamino)silane and oxygen; and
> forming a first sidewall spacer; wherein the first temperature is less than the second temperature. (emphasis added)

Chern discloses a method for forming a double-layer spacer. In particular, Chern includes the following disclosure:

> Using the gate as a doping mask, ions such as Arsenic with concentration of about 10^{13} /cm^2 are implanted into the substrate 10, generally followed by a thermal driving and annealing in a temperature of about 900-1000°C. The cross-sectional view of FIG. 4 illustrates further steps of the formation of the tetraetheoxysilane (TEOS) 20A and 20B layer with about 200 angstroms in thickness being conformably deposited on the gate. In the embodiment, a low-pressure chemical deposition is applied. Next, a silicon nitride layer 22A and 22B and a second silicon oxide 24A and 24B are formed in order on the tetraetheoxysilane (TEOS) 20A and 20B layer by chemical vapor deposition (CVD).
>
> (Chern, col. 2, lines 53 – 648, and FIG. 47)

As such, nothing in Chern teaches or suggests a deposition temperature and pressure for a silicon nitride layer formed on the TEOS, other than to disclose that chemical vapor deposition is used.

Laxman discloses a method to form silicon oxynitride films. In particular, Laxman includes the following disclosure:

> The process involves reaction of bis(tertiarybutylamino)silane with N_2O and NH_3 at 600^{0}C and 500 mTorr reactor pressure. The precursor and reactants are introduced into the heated reactor, as in Example 1. Using 60 sccm BTBAS with varying amounts of N_2O and NH_3, the film properties could be varied from a silicon nitride to various silicon oxynitrides. This is shown in the FTIR spectra normalized in FIG. 2. Here the percentages are of N_2O in the mixture of N_2O + NH_3 (total volumetric flow of 200 sccm). The average deposition rate varied from 20 to 29 Angstroms per minute, with higher rates occuring with higher percentages of N_2O. In FIG. 3, the full effect of changing the reactants is displayed. ***The temperature and pressure were maintained at 600^{0}C and 500 mTorr for these depositions***. The film refractive index then changed from near 2.0 (silicon nitride) to 1.46 (silicon oxide). This shows that a dielectric stack of oxides, nitrides, and oxynitrides may be deposited in a single reactor at a fixed temperature and pressure.
>
> (emphasis added) (Laxman, col., 8, lines 56 – 67)

As such, Laxman discloses that the silicon oxynitride film is formed at a constant temperature of 600^{0}C and a constant pressure of 500 mTorr.

It is respectfully submitted that Chern and Laxman do not teach or suggest a combination with each other. Applicant respectfully submits that it would be impermissible hindsight, based on Applicant's own disclosure to combine Chern and Laxman.

Applicant also respectfully submits that there is no motivation to combine Chern and Laxman. Chern relates to the formation of gate spacers, whereas Laxman relates to forming layers of dielectric over a substrate for the production of electronic devices such as flat panel displays. In fact, there is no disclosure in Laxman of forming sidewall spacers. As such, Applicant respectfully submits that Chern would not be motivated to look at Laxman.

Even if Chern and Laxman were somehow combined, the combination would still not include all the limitations of independent claims 1 or 11. In particular, claim 1 includes the limitation of "a second temperature in a range of 580°C to less than 600°C and a second pressure of about 65 Pascal" and claim 11 includes the limitation of "a second temperature

of between 580°C and less than 600°C and a second pressure of about 65 Pascal." The combination of Chern and Laxman does not teach these limitations. As such, applicant respectfully submits that claims 1 and 11 are patentable over the combination of Chern and Laxman under 35 U.S.C. §103(a) and request removal of the rejection.

Claims 2 – 5 and 7 – 10 depend either directly or indirectly from independent claim 1 and thus claims 2 – 5 and 7 – 10 each include the limitation of "a second temperature in a range of 580°C to less than 600°C and a second pressure of about 65 Pascal." Claims 12 – 14, 16, and 17 depend either directly or indirectly from independent claim 11 and thus claims 12 – 14, 16, and 17 each include the limitation of "a second temperature of between 580°C and less than 600°C and a second pressure of about 65 Pascal." As such, applicant respectfully submits that dependent claims 2 – 5, 7 – 10, 12 – 14, 16, and 17 are also patentable over the combination of Chern and Laxman, and request removal of the rejection under 35 U.S.C. §103(a).

Claims 15, 18 and 19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Chern and Laxman and further in view of Miles. Applicant respectfully submits that claims 15, 18, and 19 are patentable over Chern, Laxman, and Miles. Claims 15, 18, and 19 depend either directly or indirectly from independent claim 11, and thus each claim includes the limitation of "a second temperature of between 580°C and less than 600°C and a second pressure of about 65 Pascal." As discussed above, nothing in Chern or Laxman discloses this limitation.

Miles discloses a semiconductor structure having gates formed on a substrate. In particular, Miles includes the following disclosure:

> The thin gate insulator 2 is typically grown on or deposited onto the substrate 1. ***The gate insulator is typically about 30 to about 100 Å thick and can be formed by thermal oxidation of the silicon substrate at about 700 – 800 °C in the presence of dry oxygen or steam.*** A layer of conductor such as polycrystalline silicon 3 can be deposited on the gate insulator oxide. The polysilicon layer is typically

about 1500 to about 3000 Å thick and may be formed for instance by chemical-vapor deposition. The gate oxide and gate conductors can then be defined by conventional lithographic techniques. (emphasis added) (Miles, col. 2, lines 57 – 67, and FIG. 3)

The temperature range disclosed in Miles is well above the temperature range of claim 11. Moreover, there is no disclosure in Miles of a pressure for the formation of the gate insulator. As such, Miles fails to cure the deficiency of Chern and Laxman. As such, Applicant respectfully submits that because the combination of Chern, Laxman, and Miles do not include all the limitations of claim 11, dependent claims 15, 18, and 19 are patentable over the combination and request removal of the rejection.

In conclusion, Applicant respectfully submits that in view of the arguments set forth herein, the applicable rejections have been overcome. If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Suk Lee at (408) 720-8300. If there are any additional charges, please charge our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: December 9, 2004

Suk S. Lee
Attorney for Applicant
Registration No. 47,745

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1030
(408) 720-8300